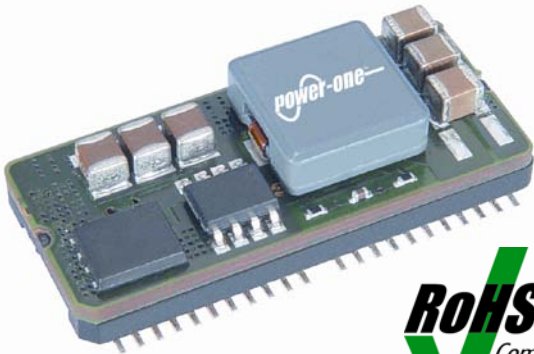


Member of the **maxVZ** Family



Applications

- Low voltage, high density systems with Intermediate Bus Architectures (IBA)
- Point-of-load regulators for high performance DSP, FPGA, ASIC, and microprocessor applications
- Industrial computing, servers, and storage
- Broadband, networking, optical, and wireless communications systems
- Active memory bus terminators

Benefits

- Integrates digital power conversion with intelligent power management
- Eliminates the need for external power management components and communication bus
- Completely programmable via pin strapping and external R and C
- One part that covers all applications
- Reduces board space, system cost and complexity, and time to market

Description

Power-One's point-of-load converters are recommended for use with regulated bus converters in an Intermediate Bus Architecture (IBA). The ZY1015 is an intelligent, fully programmable step-down point-of-load DC-DC module integrating digital power conversion and intelligent power management. The ZY1015 completely eliminates the need for external components for sequencing, tracking, protection, monitoring, and reporting. Performance parameters of the ZY1015 are programmable by pin strapping and external resistor and capacitor and can be changed by a user at any time during product development and service without a need for a communication bus.

Features

- RoHS lead free and lead-solder-exempt products are available
- Wide input voltage range: 3V–14V
- High continuous output current: 15A
- Wide programmable output voltage range: 0.5V–5.5V
- Active digital current share
- Output voltage margining
- Overcurrent and overtemperature protections
- Overvoltage and undervoltage protections, and Power Good signal tracking the output voltage setpoint
- Programmable power-up delay
- Tracking during turn-on and turn-off with guaranteed slew rates
- Sequenced and cascaded modes of operation
- Single-wire line for frequency synchronization between multiple POLs
- Programmable interleave
- Programmable feedback loop compensation
- Enable control with programmable polarity
- Flexible fault management and propagation
- Start-up into the load pre-biased up to 100%
- Full rated current sink
- Real time current and temperature measurements, monitoring, and reporting
- Small footprint SMT package: 16x32mm
- Low profile of 8mm
- Compatible with conventional pick-and-place equipment
- Wide operating temperature range
- UL 60950-1/CSA 22.2 No. 60950-1-07 Second Edition, IEC 60950-1: 2005, and EN 60950-1:2006

Reference Documents

No-Bus™ POL Converters. Z-1000 Series Application Note
Z-One® POL Converters. Eutectic Solder Process Application Note
Z-One® POL Converters. Lead-Free Process Application Note

1. Ordering Information

| ZY | 10 | 15 | y | - | zz |
|--|--|-------------------------------|--|-------------|---|
| Product family: Z-One Module | Series: No-Bus POL Converter | Output Current: 15A | RoHS compliance: No suffix - RoHS compliant with Pb solder exemption ¹ G - RoHS compliant for all six substances | Dash | Packaging Option²: T1 – 500pcs T&R T2 – 100pcs T&R T3 – 50pcs T&R Q1 – 1pc sample for evaluation only K1 – 1pc mounted on the evaluation board ³ |

¹ The solder exemption refers to all the restricted materials except lead in solder. These materials are Cadmium (Cd), Hexavalent chromium (Cr6+), Mercury (Hg), Polybrominated biphenyls (PBB), Polybrominated diphenylethers (PBDE), and Lead (Pb) used anywhere except in solder.

² Packaging option is used only for ordering and not included in the part number printed on the POL converter label.

³ The evaluation board is available in only one configuration: ZY1015-K1.

Example: **ZY1015G-T3**: A 50-piece reel of RoHS compliant POL converters. Each POL converter is labeled ZY1015G.

2. Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the POL converter.

| Parameter | Conditions/Description | Min | Max | Units |
|-----------------------|--------------------------------------|-----|-----|-------|
| Operating Temperature | Controller Case Temperature | -40 | 105 | °C |
| Input Voltage | 250ms Transient | | 15 | VDC |
| Output Current | (See Output Current Derating Curves) | -15 | 15 | ADC |

3. Environmental and Mechanical Specifications

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|----------------------------|--|---|-----|------------|----------|
| Ambient Temperature Range | | -40 | | 85 | °C |
| Storage Temperature (Ts) | | -55 | | 125 | °C |
| Weight | | | | 15 | grams |
| MTBF | Calculated Per Telcordia Technologies SR-332 | 4.82 | | | MHrs |
| Peak Reflow Temperature | ZY1015 ZY1015G | | 245 | 220 260 | °C °C |
| Lead Plating | ZY1015 and ZY1015G | 100% Matte Tin or 1.5µm Ag over 1.5µm Ni | | | |
| Moisture Sensitivity Level | ZY1015 ZY1015G | | | 2 3 | |

4. Electrical Specifications

Specifications apply at the input voltage from 3V to 14V, output load from 0 to 15A, ambient temperature from -40°C to 85°C, output capacitance consisting of 110µF ceramic and 220µF tantalum, and default performance parameters settings unless otherwise noted.

4.1 Input Specifications

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|--|--|------|------|-----|-------|
| Input voltage (V_{IN}) | At $V_{IN} < 4.75V$, VLDO pin needs to be connected to an external voltage source higher than 4.75V | 3 | | 14 | VDC |
| Input Current (at no load) | $V_{IN} \geq 4.75V$, VLDO pin connected to V_{IN} | | 50 | | mADC |
| Undervoltage Lockout (VLDO connected to V_{IN}) | Ramping Up | | 4.00 | | VDC |
| | Ramping Down | | 3.9 | | VDC |
| Undervoltage Lockout (VLDO connected to $V_{AUX}=5V$) | Ramping Up | | 2.8 | | VDC |
| | Ramping Down | | 2.7 | | VDC |
| External Low Voltage Supply | Connect to VLDO pin when $V_{IN} < 4.75V$ | 4.75 | | 14 | VDC |
| VLDO Input Current | Current drawn from the external low voltage supply at VLDO=5V | | 50 | | mADC |

4.2 Output Specifications

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|---|--|--|-----------|-----|------------------|
| Output Current (I_{OUT}) | $V_{IN\ MIN}$ to $V_{IN\ MAX}$ | -15 ¹ | | 15 | ADC |
| Output Voltage Range (V_{OUT}) | Programmable ² with a resistor between TRIM and REF pins Default (no resistor) | 0.5 | | 5.5 | VDC |
| | | | 0.5 | | VDC |
| Output Voltage Setpoint Accuracy ³ | $V_{IN}=12V$, $I_{OUT}=0.5 \cdot I_{OUT\ MAX}$, room temperature | $\pm 1.5\%$ or 20mV whichever is greater | | | % V_{OUT} |
| Line Regulation ³ | $V_{IN\ MIN}$ to $V_{IN\ MAX}$ | | ± 0.2 | | % V_{OUT} |
| Load Regulation ³ | 0 to $I_{OUT\ MAX}$ | | ± 0.2 | | % V_{OUT} |
| Dynamic Regulation Peak Deviation Peak Deviation Settling Time | Slew rate 1A/ μs , 50-75% load step, $V_{IN} \geq 5V$ $V_{IN} = 3.3V$ to 10% of peak deviation | | 80 | | mV |
| | | | 100 | | mV |
| | | | 30 | | μs |
| Output Voltage Peak-to-Peak Ripple and Noise Full Load | $V_{IN}=5.0V$, $V_{OUT} \leq 2.5V$ $V_{IN}=5.0V$, $V_{OUT} > 2.5V$ $V_{IN}=12V$, $V_{OUT} \leq 2.5V$ $V_{IN}=12V$, $V_{OUT} > 2.5V$ | | 15 | | mV |
| | | | 25 | | mV |
| | | | 25 | | mV |
| | | | 30 | | mV |
| Temperature Coefficient | $V_{IN}=12V$, $I_{OUT}=0.5 \cdot I_{OUT\ MAX}$ | | 100 | | ppm/ $^{\circ}C$ |
| Switching Frequency | | 450 | 500 | 550 | kHz |

¹ At the negative output current (bus terminator mode) efficiency of the ZY1015 degrades resulting in increased internal power dissipation. Therefore maximum allowable negative current under specific conditions is 20% lower than the current determined from the derating curves shown in paragraph 5.5.

² ZY1015 is a step-down converter, thus the output voltage is always lower than the input voltage as show in Figure 1.

³ Digital PWM has an inherent quantization uncertainty of $\pm 6.25mV$ that is not included in the specified static regulation parameters.

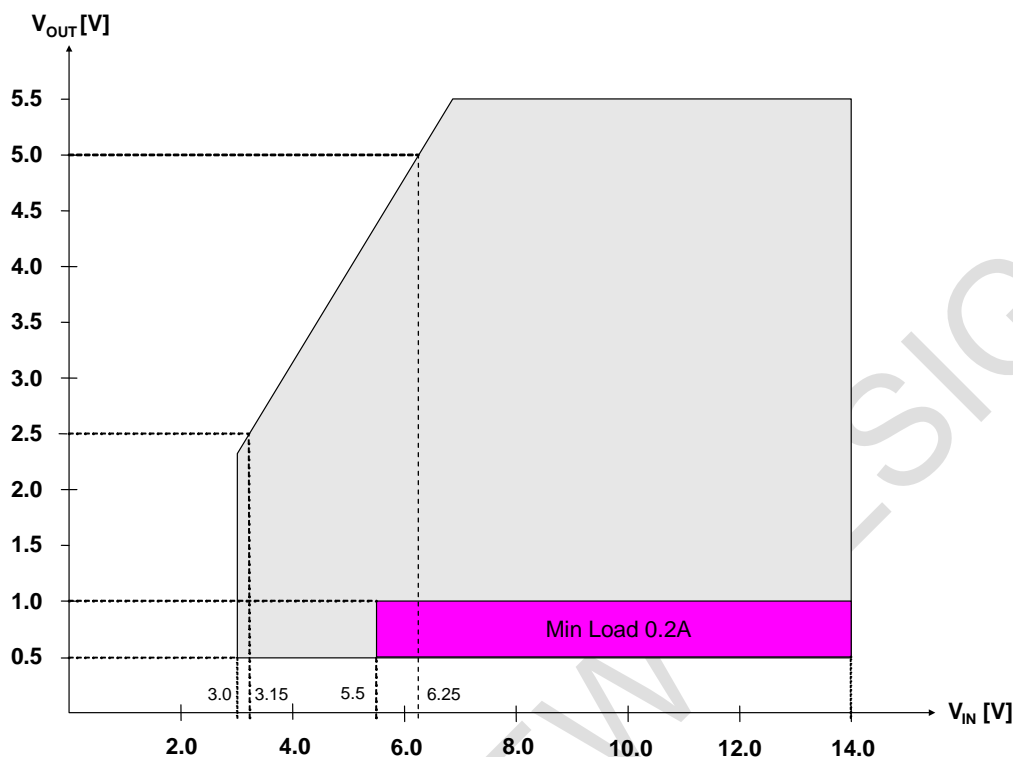


Figure 1. Output Voltage as a Function of Input Voltage and Output Current

4.3 Protection Specifications

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|---------------------------------------|---|----------------------------|------------------|-----|-----------------------|
| Output Overcurrent Protection | | | | | |
| Type | | Non-Latching, 130ms period | | | |
| Threshold | | | 170 | | %I _{OUT} |
| Threshold Accuracy | | -25 | | 25 | %I _{OCP.SET} |
| Output Overvoltage Protection | | | | | |
| Type | | Latching | | | |
| Threshold | Follows the output voltage setpoint | | 130 ¹ | | %V _{O.SET} |
| Threshold Accuracy | Measured at V _{O.SET} =2.5V | -2 | | 2 | %V _{OVP.SET} |
| Delay | From instant when threshold is exceeded until the turn-off command is generated | | 6 | | μs |
| Output Undervoltage Protection | | | | | |
| Type | | Non-Latching, 130ms period | | | |
| Threshold | Follows the output voltage setpoint | | 75 | | %V _{O.SET} |
| Threshold Accuracy | Measured at V _{O.SET} =2.5V | -2 | | 2 | %V _{UVP.SET} |
| Delay | From instant when threshold is exceeded until the turn-off command is generated | | 6 | | μs |

| Overtemperature Protection | | | | | |
|-------------------------------|--|----------------------------|-------------|---|---------------|
| Type | | Non-Latching, 130ms period | | | |
| Turn Off Threshold | Temperature is increasing | | 120 | | °C |
| Turn On Threshold | Temperature is decreasing after module was shut down by OTP | | 110 | | °C |
| Threshold Accuracy | | -5 | | 5 | °C |
| Delay | From instant when threshold is exceeded until the turn-off command is generated | | 6 | | µs |
| Power Good Signal (PGOOD pin) | | | | | |
| Logic | V_{OUT} is inside the PG window and stable V_{OUT} is outside of the PG window or ramping up/down | | High Low | | N/A |
| Lower Threshold | Follows the output voltage setpoint | | 90 | | % $V_{O,SET}$ |
| Upper Threshold | Follows the output voltage setpoint | | 110 | | % $V_{O,SET}$ |
| Delay | From instant when threshold is exceeded until status of PG signal changes | | 6 | | µs |
| Threshold Accuracy | Measured at $V_{O,SET}=2.5V$ | -2 | | 2 | % $V_{O,SET}$ |

¹ Minimum OVP threshold is 1.0V

4.4 Feature Specifications

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|---|--|---------------------|------|--------|-------------|
| Current Share (CS pin) | | | | | |
| Type | | Active, Single Line | | | |
| Maximum Number of Modules Connected in Parallel | $I_{OUT\ MIN} \geq 20\% * I_{OUT\ NOM}$ | | 10 | | |
| Maximum Number of Modules Connected in Parallel | $I_{OUT\ MIN} = 0$ | | 4 | | |
| Current Share Accuracy | $I_{OUT\ MIN} \geq 20\% * I_{OUT\ NOM}$ | | | ±20 | % I_{OUT} |
| Interleave (IM and INTL0...INTL4 pins) | | | | | |
| Interleave (Phase Lag) | Programmable via INTL0...INTL4 pins in 11.25° steps (IM pin is open) | 0 | | 348.75 | degree |
| | Default (IM pin is pulled low) | | 0 | | degree |
| Sequencing (DELAY pin) | | | | | |
| Power-Up Delay | Programmable by capacitor connected to DELAY pin | | | 210 | ms |
| | Default: $C_{DELAY}=0$ | | 0 | | ms |
| Tracking | | | | | |
| Rising Slew Rate | Proportional to SYNC frequency | | 0.1 | | V/ms |
| Falling Slew Rate | Proportional to SYNC frequency | | -0.5 | | V/ms |

| Enable (EN and ENP pins) | | | | | |
|---|--|--|----------------|-----------------|-------------------|
| EN Pin Polarity | ENP pin is pulled low | Negative (enables the output when EN pin is pulled low) | | | |
| | ENP pin is open | Positive (enables the output when EN pin is open or pulled high) | | | |
| EN High Threshold | | 2.3 | | | VDC |
| EN Low Threshold | | | | 1.0 | VDC |
| Open Circuit Voltage | EN and ENP | | 3.3 | | VDC |
| Turn-On Delay | From EN pin changing state to V _{OUT} starting to ramp up | | 0 | | ms |
| Turn-Off Delay | From EN pin changing state to V _{OUT} reaching 0V | | 11 | | ms |
| Feedback Loop Compensation (CCA0...CCA2 pins) | | | | | |
| CCA=7 (default) | Recommended V _{IN} range | 8 | 12 | 14 | VDC |
| | Recommended C _{OUT} /ESR range, combination of ceramic+ tantalum | 50/5 + 220/40 | 100/5 + 470/40 | 400/5 + 2000/20 | μF/mΩ μF/mΩ |
| CCA=6 | Recommended V _{IN} range | 8 | 12 | 14 | VDC |
| | Recommended C _{OUT} range, tantalum Recommended ESR range, tantalum | 440 40 | 880 25 | 10,000 10 | μF mΩ |
| CCA=5 | Recommended V _{IN} range | 8 | 12 | 14 | VDC |
| | Recommended C _{OUT} /ESR range, ceramic | 100/5 | 220/5 | 400/5 | μF/mΩ |
| CCA=3 or CCA=4 | Recommended V _{IN} range | 3 | 5 | 5.5 | VDC |
| | Recommended C _{OUT} /ESR range, combination of ceramic + tantalum | 50/5 + 220/40 | 100/5 + 470/40 | 200/5 + 880/40 | μF/mΩ μF/mΩ |
| CCA=2 | Recommended V _{IN} range | 3 | 5 | 5.5 | VDC |
| | Recommended C _{OUT} /ESR range, tantalum | 100/25 | 440/20 | 1,000/10 | μF/mΩ |
| CCA=1 | Recommended V _{IN} range | 3 | 5 | 5.5 | VDC |
| | Recommended C _{OUT} /ESR range, ceramic | 100/5 | 220/5 | 400/5 | μF/mΩ |
| CCA=0 | Recommended V _{IN} range | 6 | | 11 | VDC |
| | Recommended C _{OUT} /ESR range, combination of ceramic+ tantalum | 50/5 + 220/40 | 100/5 + 470/40 | 200/5 + 880/40 | μF/mΩ μF/mΩ |
| Output Current Monitoring (CS pin) | | | | | |
| Output Current Monitoring Accuracy | 20%*I _{OUT NOM} < I _{OUT} < I _{OUT NOM} V _{IN} =12V | -20 | | +20 | %I _{OUT} |
| Conversion Ratio | Duty Cycle of the negative pulse corresponding to 100% of nominal current | | 65 | | % |
| Temperature Monitoring (TEMP pin) | | | | | |
| Temperature Monitoring Accuracy | Junction temperature of POL controller | -5 | | +5 | °C |
| Conversion Ratio | Junction temperature from -40°C to 140°C | | 10 | | mV/°C |
| Monitoring Voltage Range | Corresponds to -40°C to 140°C junction temperature range | 0.2 | | 2 | VDC |
| Output Impedance | TEMP pin | | 6.4 | | kΩ |
| Remote Voltage Sense (-VS and +VS pins) | | | | | |
| Type | | Differential | | | |
| Voltage Drop Compensation | Between +VS and V _{OUT} | | | 300 | mV |
| Voltage Drop Compensation | Between -VS and PGND | | | 100 | mV |

4.5 Signal Specifications

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|--|--|------------|-----|------------|------------------|
| VDD | Internal supply voltage | 3.15 | 3.3 | 3.45 | V |
| SYNC Line | | | | | |
| ViL_s | LOW level input voltage | -0.5 | | 0.3 x VDD | V |
| ViH_s | HIGH level input voltage | 0.75 x VDD | | VDD + 0.5 | V |
| Vhyst_s | Hysteresis of input Schmitt trigger | 0.25 x VDD | | 0.45 x VDD | V |
| IoL_s | LOW level sink current V(SYNC)=0.5V | 14 | | 60 | mA |
| Ipu_s | Pull-up current source V(SYNC)=0V | 300 | | 1000 | μA |
| Tr_s | Maximum allowed rise time 10/90%VDD | | | 300 | ns |
| Cnode_s | Added node capacitance | | 5 | 10 | pF |
| Freq_s | Clock frequency of external SYNC line | 475 | | 525 | kHz |
| Tsynq | Sync pulse duration | 22 | | 28 | % of clock cycle |
| T0 | Data=0 pulse duration | 72 | | 78 | % of clock cycle |
| Inputs: INTL0...INTL4, CCA0...CCA2, EN, ENP, IM | | | | | |
| Iup_x | Pull-up current source V(X)=0 | 25 | | 110 | μA |
| ViL_x | LOW level input voltage | -0.5 | | 0.3 x VDD | V |
| ViH_x | HIGH level input voltage | 0.7 x VDD | | VDD+0.5 | V |
| Vhyst_x | Hysteresis of input Schmitt trigger | 0.1 x VDD | | 0.3 x VDD | V |
| RdnL_x | External pull down resistance pin forced low | | | 10 | kΩ |
| Power Good and OK Inputs/Outputs | | | | | |
| Iup_PG | Pull-up current source V(PG)=0 | 25 | | 110 | μA |
| Iup_OK | Pull-up current source V(OK)=0 | 175 | | 725 | μA |
| ViL_x | LOW level input voltage | -0.5 | | 0.3 x VDD | V |
| ViH_x | HIGH level input voltage | 0.7 x VDD | | VDD+0.5 | V |
| Vhyst_x | Hysteresis of input Schmitt trigger | 0.1 x VDD | | 0.3 x VDD | V |
| IoL_x | LOW level sink current at 0.5V | 4 | | 20 | mA |
| Current Share/Sense Bus | | | | | |
| Iup_CS | Pull-up current source at V(CS)=0V | 0.84 | | 3.10 | mA |
| ViL_CS | LOW level input voltage | -0.5 | | 0.3 x VDD | V |
| ViH_CS | HIGH level input voltage | 0.75 x VDD | | VDD+0.5 | V |
| Vhyst_CS | Hysteresis of input Schmitt trigger | 0.25 x VDD | | 0.45 x VDD | V |
| IoL_CS | LOW level sink current V(CS)=0.5V | 14 | | 60 | mA |
| Tr_CS | Maximum allowed rise time 10/90% VDD | | | 100 | ns |

5. Typical Performance Characteristics

5.1 Efficiency Curves

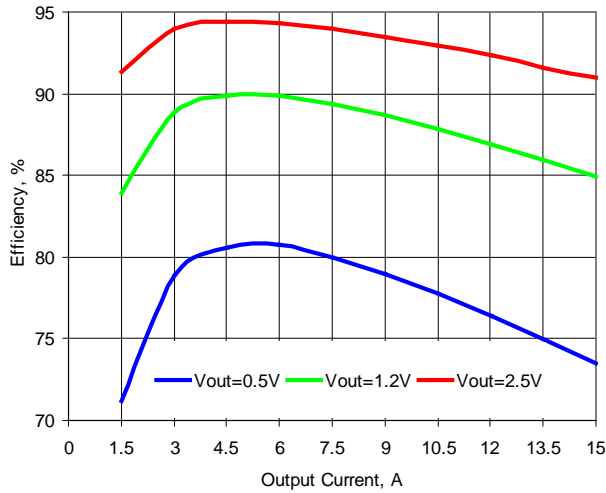


Figure 2. Efficiency vs. Load. Vin=3.3V

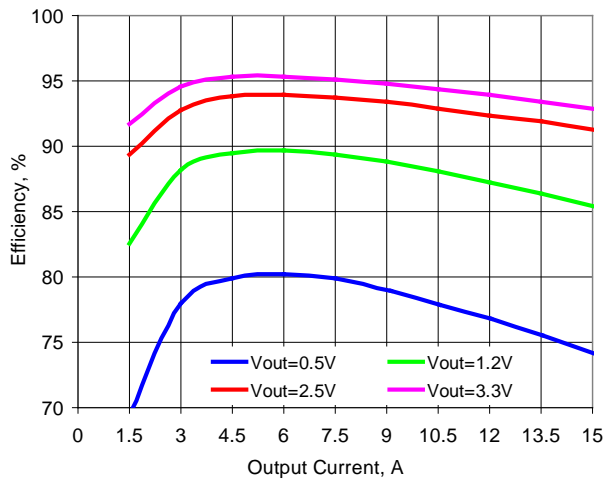


Figure 3. Efficiency vs. Load. Vin=5V

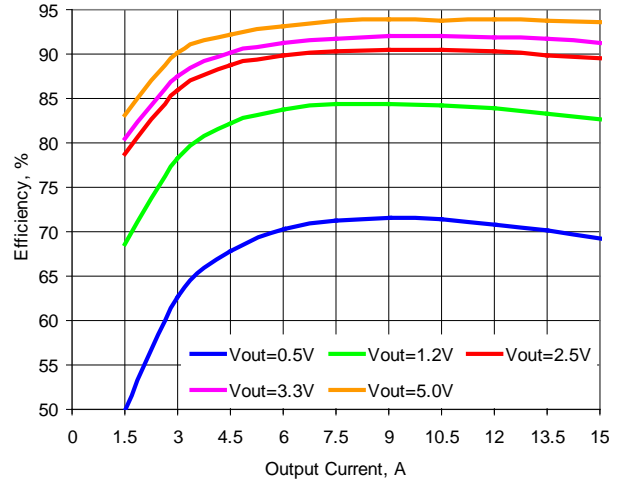


Figure 4. Efficiency vs. Load. Vin=12V

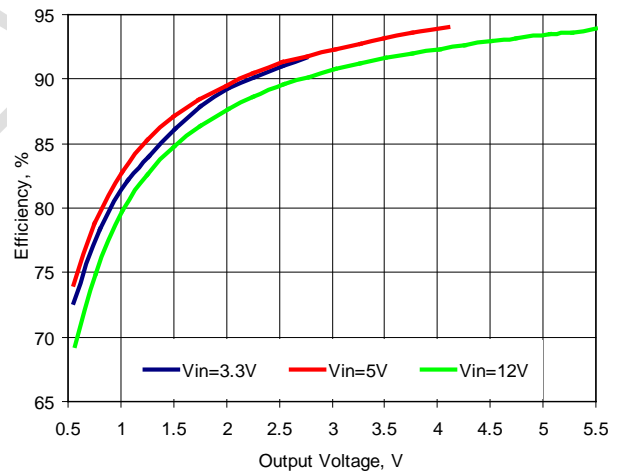


Figure 5. Efficiency vs. Output Voltage, Iout=15A

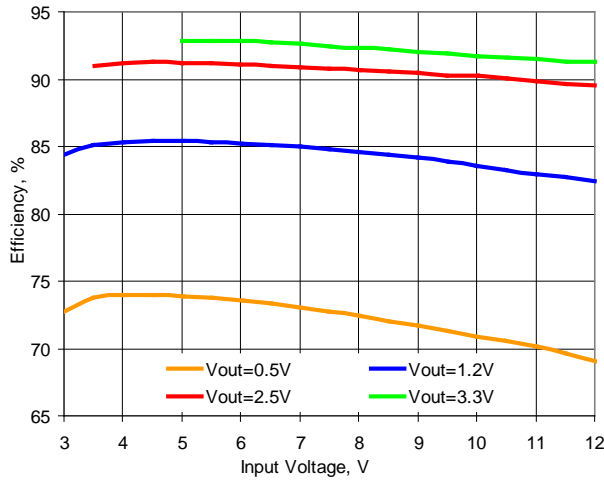


Figure 6. Efficiency vs. Input Voltage. I_{out}=15A

5.2 Turn-On Characteristics

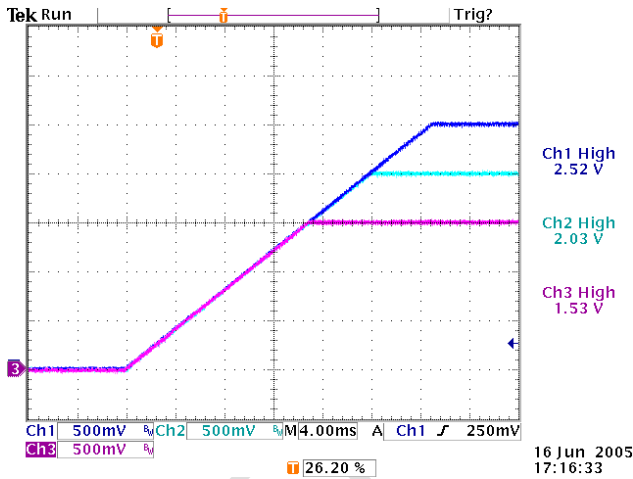


Figure 7. Tracking Turn-On.
V_{in}=12V, Ch1 – V1, Ch2 – V2, Ch3 – V3

5.3 Turn-Off Characteristics

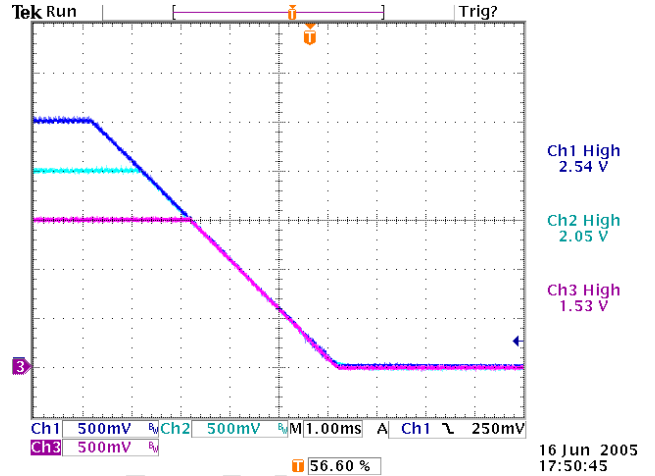


Figure 8. Tracking Turn-Off
V_{in}=12V, Ch1 – V1, Ch2 – V2, Ch3 – V3

5.4 Transient Response

The pictures below show the deviation of the output voltage in response to the 50-75-50% step load at 1.0A/μs. In all tests the POL converters had 5x22μF ceramic capacitors and a 220μF tantalum capacitor connected across the output pins. The speed of the transient response was optimized by selecting appropriate CCA settings.

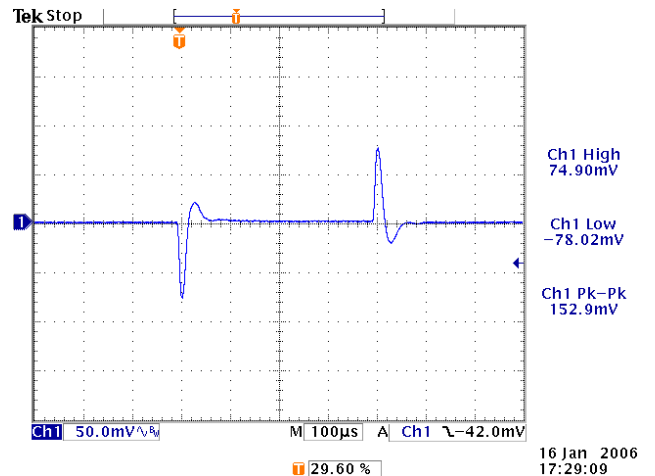


Figure 9. V_{in}=12V, V_{out}=1V. CCA=07

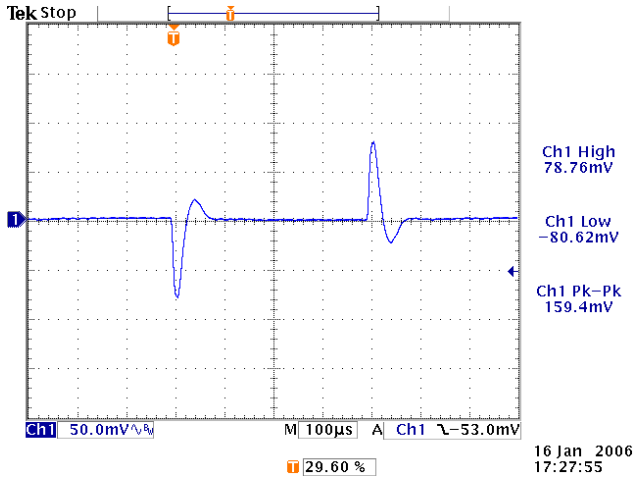


Figure 10. Vin=12V, Vout=2.5V. CCA=05

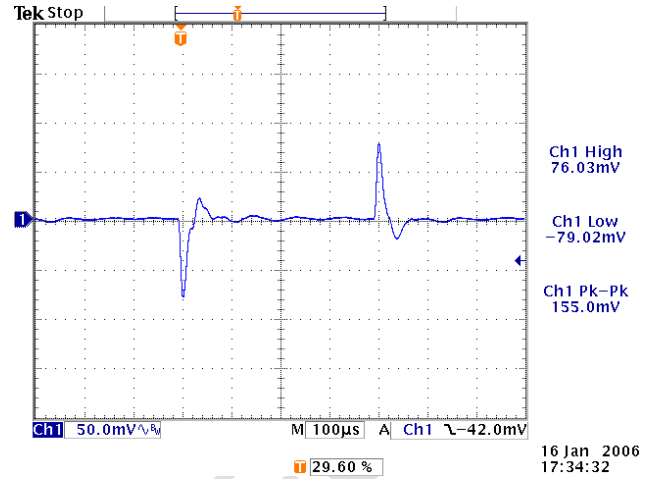


Figure 13. Vin=5V, Vout=2.5V. CCA=03

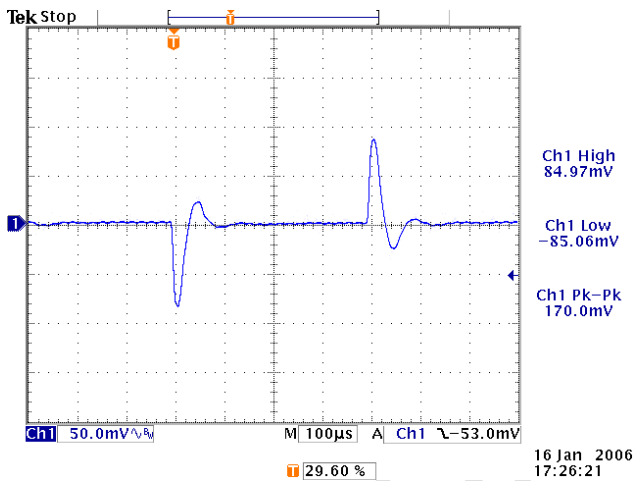


Figure 11. Vin=12V, Vout=5V, CCA=05

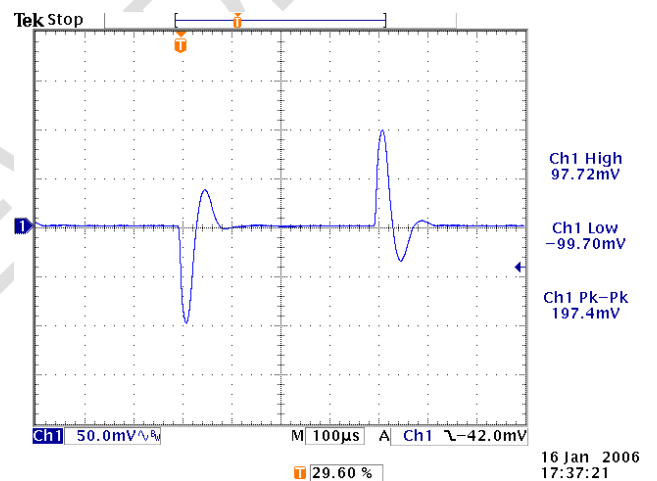


Figure 14. Vin=3.3V, Vout=1V. CCA=03

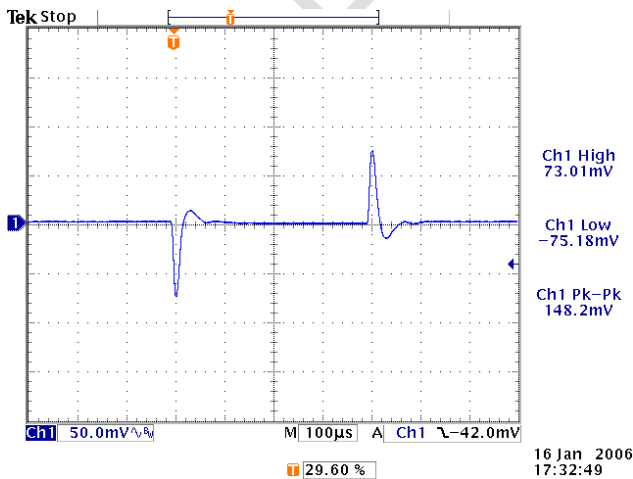


Figure 12. Vin=5V, Vout=1V. CCA=03

5.5 Thermal Derating Curves

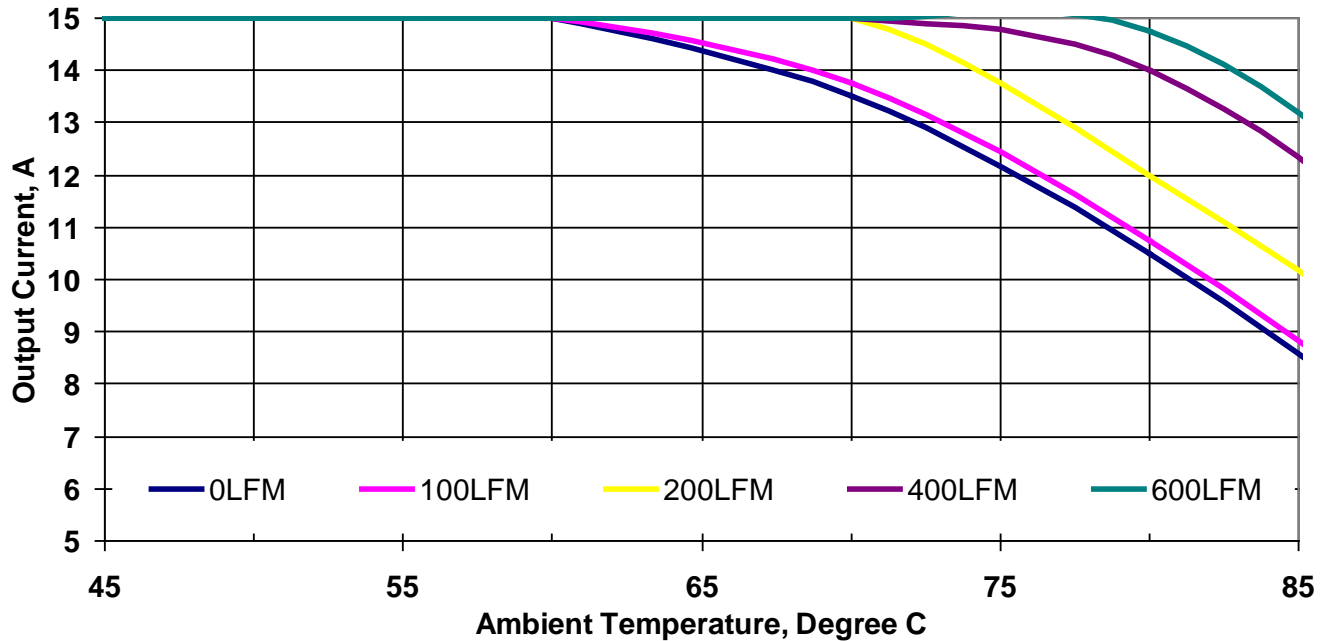


Figure 15. Thermal Derating Curves. Vin=12V, Vout=5.0V

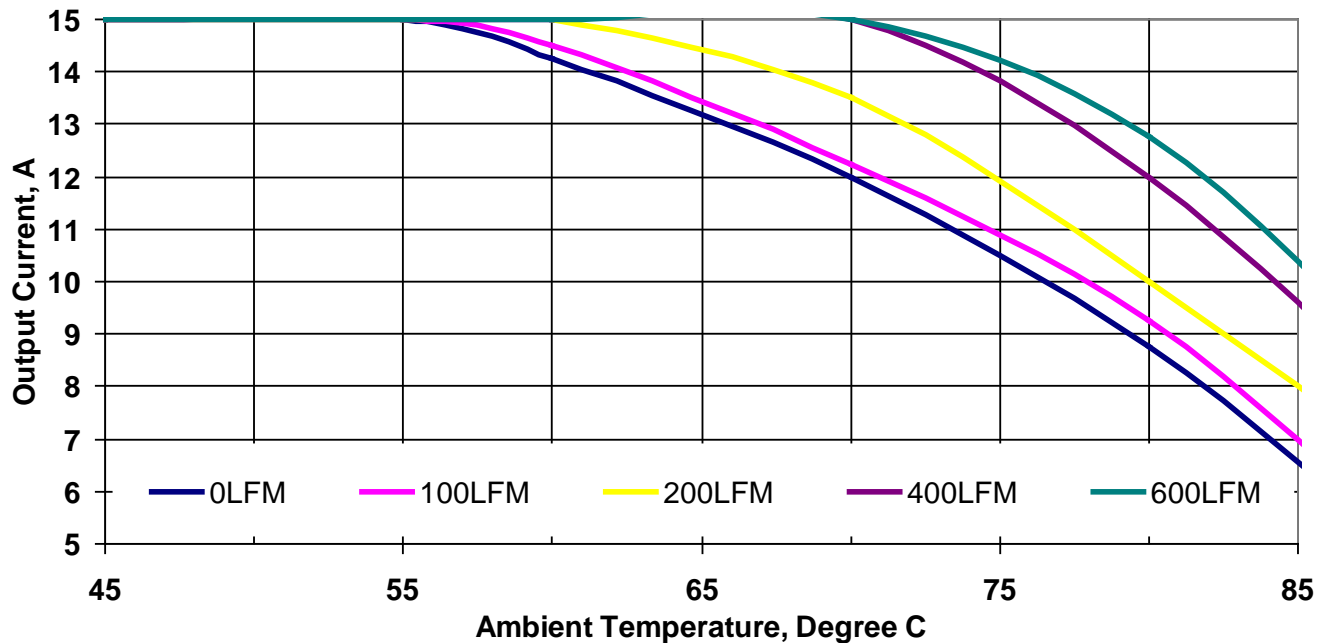


Figure 16. Thermal Derating Curves. Vin=14V, Vout=5.0V

6. Typical Application

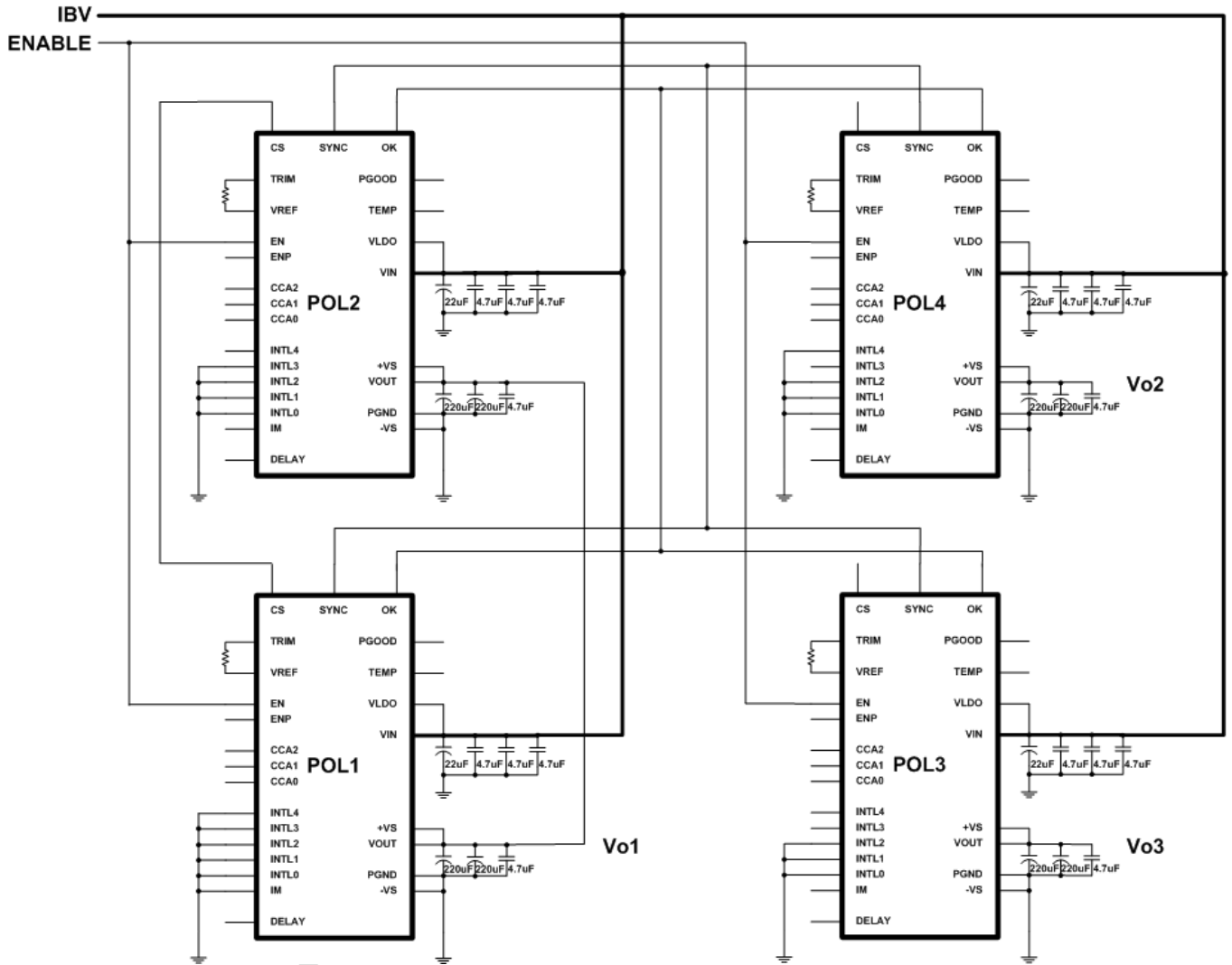


Figure 17. Complete Schematic of Application with Three Independent Outputs. Intermediate Bus Voltage is from 8V to 14V.

In this application four POL converters are configured to deliver three independent output voltages. POL1 and POL2 are connected in parallel for increased output current. Output voltages are programmed with the resistors connected between TRIM and VREF pins of individual converters.

POL1 is configured as a master (IM and INTL0...INTL4 pins are grounded) and all other POL converters are synchronized to the switching frequency of POL1. Interleave is programmed with pins INTL0...INTL4 to ensure the lowest input and output noise. POL2 has 180° phase shift, POL 3 and POL4 have phase shifts of 270° and 90° respectively.

All converters are controlled by the common ENABLE signal. Turn-on and turn-off processes of the system are illustrated by pictures in Figure 7 and Figure 8.

7. Pin Assignments and Description

| Pin Name | Pin No. | Pin Type | Buffer Type | Pin Description | Notes |
|----------|---------|----------|-------------|--|---|
| VLDO | 1 | P | | Low Voltage Dropout | Connect to an external voltage source higher than 4.75V, if $V_{IN} < 4.75V$. Connect to V_{IN} , if $V_{IN} \geq 4.75V$ |
| IM | 2 | I | PU | Interleave Mode | Tie to PGND for master or leave open to set interleave by INTL0...INTL4 pins |
| TEMP | 3 | A | | Temperature Measurement | Analog voltage proportional to junction temperature of the controller |
| ENP | 4 | I | PU | Enable Logic Selection | Tie to PGND for Negative logic or leave open for Positive logic |
| DELAY | 5 | A | | Power-Up Delay | Connect a capacitor between the pin and PGND to program the Power-Up delay. Leave open for zero delay |
| CCA2 | 6 | I | PU | Compensation Coefficient Address Bit 2 | Tie to PGND for 0 or leave open for 1 |
| CCA1 | 7 | I | PU | Compensation Coefficient Address Bit 1 | Tie to PGND for 0 or leave open for 1 |
| CCA0 | 8 | I | PU | Compensation Coefficient Address Bit 0 | Tie to PGND for 0 or leave open for 1 |
| VREF | 9 | A | | Voltage Reference | To program the output voltage, connect a resistor between VREF and TRIM |
| EN | 10 | I | PU | Enable | Polarity is determined by ENP pin |
| OK | 11 | I/O | PU | Fault Status | Connect to OK pin of other Z-1000 POLs. Leave open, if not used |
| SYNC | 12 | I/O | PU | Frequency Synchronization Line | Connect to SYNC pin of other Z-POLs and/or to an external clock generator |
| PGOOD | 13 | I/O | PU | Power Good | |
| TRIM | 14 | A | | Output Voltage Trim | To program the output voltage, connect a resistor between VREF and TRIM |
| CS | 15 | I/O | PU | Current Share/Sense | Connect to CS pin of other Z-POLs connected in parallel |
| INTL4 | 16 | I | PU | Interleave Bit 4 | Tie to PGND for 0 or leave open for 1 |
| INTL3 | 17 | I | PU | Interleave Bit 3 | Tie to PGND for 0 or leave open for 1 |
| INTL2 | 18 | I | PU | Interleave Bit 2 | Tie to PGND for 0 or leave open for 1 |
| INTL1 | 19 | I | PU | Interleave Bit 1 | Tie to PGND for 0 or leave open for 1 |
| INTL0 | 20 | I | PU | Interleave Bit 0 | Tie to PGND for 0 or leave open for 1 |
| -VS | 21 | I | PU | Negative Voltage Sense | Connect to the negative point close to the load |
| +VS | 22 | I | PU | Positive Voltage Sense | Connect to the positive point close to the load |
| VOUT | 23 | P | | Output Voltage | |
| PGND | 24 | P | | Power Ground | |
| VIN | 25 | P | | Input Voltage | |

Legend: I=input, O=output, I/O=input/output, P=power, A=analog, PU=internal pull-up

8. Pin and Feature Description

8.1 VLDO, Low Voltage Dropout

The input of the internal linear regulator. V_{VLDO} always needs to be greater than 4.75V for normal operation of the POL converter.

8.2 IM, Interleave Mode

The input with the internal pull-up resistor. When the pin is left floating, the phase lag of the POL converter is set by INTL0...INTL4 pins. If the pin is pulled low, the phase lag is set to 0°. Pulling all INTL pins and the IM pin low configures a POL converter as a master. The master determines the clock on the SYNC line.

8.3 TEMP, Temperature Measurement

The voltage output of the internal temperature sensor measuring junction temperature of the controller IC. Voltage range from 0 to 2V corresponds to the temperature range from -50°C to 150°C.

8.4 ENP, Enable Polarity

The input with the internal pull-up resistor. When the ENP pin is pulled low, the control logic of the EN input is inverted.

8.5 DELAY, Power-Up Delay

The input of the POR circuit with the internal pull-up resistor. By connecting a capacitor between the pin and PGND the power-up delay can be programmed.

8.6 CCA[0:2], Compensation Coefficient Address

Inputs with internal pull-ups to select one of 7 sets of digital filter coefficients optimized for various application conditions.

8.7 VREF, Voltage Reference

The output of the 2V internal voltage reference that is used to program the output voltage of the POL converter.

8.8 EN, Enable

The input with the internal pull-up resistor. The POL converter is turned off, when the pin is pulled low (see ENP to inverse logic of the Enable function).

8.9 OK, Fault Status

The open drain input/output with the internal pull-up resistor. The POL converter pulls its OK pin low, if a

fault occurs. Pulling low the OK input by an external circuitry turns off the POL converter.

8.10 SYNC, Frequency Synchronization Line

The bidirectional input/output with the internal pull-up resistor. If the POL converter is configured as a master, the SYNC line propagates clock to other POL converters. If the POL converter is configured as a slave, the internal clock recovery circuit synchronizes the POL converter to the clock of the SYNC line.

8.11 PG, Power Good

The open drain input/output with the internal pull-up resistor. The pin is pulled low by the POL converter, if the output voltage is outside of the window defined by the Power Good High and Low thresholds.

Note: See the No-Bus Application Note for recommendations on PG deglitching.

8.12 TRIM, Output Voltage Trim

The input of the TRIM comparator for the output voltage programming.

The output voltage can be programmed by a single resistor connected between VREF and TRIM pins. Resistance of the trim resistor can be determined from the equation below:

$$R_{TRIM} = \frac{20 \times (5.5 - V_{OUT})}{V_{OUT}}, \text{ k}\Omega$$

where V_{OUT} is the desired output voltage in Volts.

If the R_{TRIM} is open or the TRIM pin is shorted to PGND, the $V_{OUT}=0.5V$.

8.13 CS, Current Share/Sense Bus

The open drain digital input/output with the internal pull-up resistor. The duty cycle of the digital signal is proportional to the output current of the POL converter. External capacitive loading of the pin shall be avoided.

8.14 INTL[0:4], Interleave Bits

Inputs with internal pull-up resistors. The encoded address determines the phase lag of the POL converter when the IM pin is left floating. One digit of the address corresponds to the phase lag of 11.25°.

Note: Due to noise sensitivity issues that may occur in limited cases, it is recommended to avoid phase lag settings of 112.5 and 123.75 degrees, otherwise false PG and/or OV indications may occur.

8.15 -VS and +VS

The differential voltage input of the POL converter feedback loop.

9. Application Information

9.1 Output Voltage Margining

Margining can be implemented either by changing the trim voltage as described in the previous paragraph or by changing the resistance between the REF and TRIM pins.

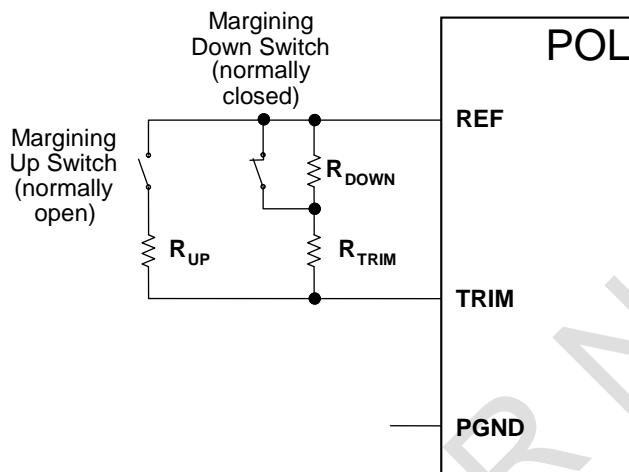


Figure 18. Margining Configuration

In the schematic shown in Figure 18, the nominal output voltage is set with the trim resistor R_{TRIM} calculated from the equation in the paragraph 8.12. Resistors R_{UP} and R_{DOWN} are added to margin the output voltage up and down respectively and determined from the equations below.

$$R_{UP} = \frac{20 \times R_{TRIM}}{20 + R_{TRIM}} \times \left(\frac{5 \times R_{TRIM} - \Delta V\%}{\Delta V\%} \right), \text{ k}\Omega$$

$$R_{DOWN} = (20 + R_{TRIM}) \times \left(\frac{\Delta V\%}{100 - \Delta V\%} \right), \text{ k}\Omega$$

where R_{TRIM} is the value of the trim resistor in $\text{k}\Omega$ and $\Delta V\%$ is the absolute value of desired margining expressed in percents of the nominal output voltage.

During normal operation the resistors are removed from the circuit by the switches. The “Margining Down” switch is normally closed shorting the resistor R_{DOWN} while the “Margining Up” switch is normally open disconnecting the resistor R_{UP} .

An alternative configuration of the margining circuit is shown in Figure 19. In the configuration both switches are normally open that may be advantageous in some implementations.

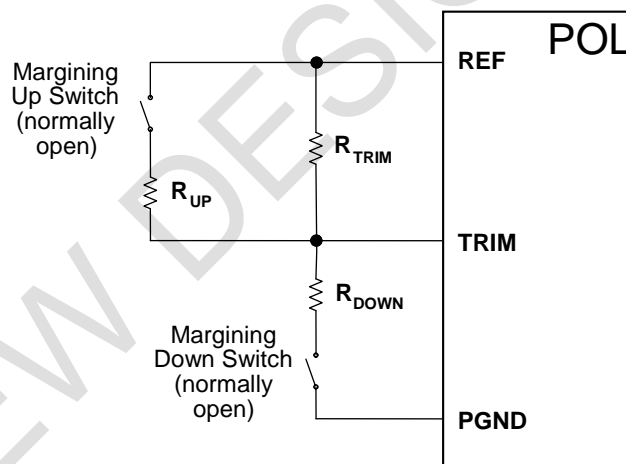


Figure 19. Alternative Margining Configuration

R_{UP} and R_{DOWN} for this configuration are determined from the following equations:

$$R_{UP} = \frac{20 \times R_{TRIM}}{20 + R_{TRIM}} \times \left(\frac{5 \times R_{TRIM} - \Delta V\%}{\Delta V\%} \right), \text{ k}\Omega$$

$$R_{DOWN} = \frac{20 \times R_{TRIM}}{20 + R_{TRIM}} \times \left(\frac{100 - \Delta V\%}{\Delta V\%} \right), \text{ k}\Omega$$

Caution: Noise injected into the TRIM node may affect accuracy of the output voltage and stability of the POL converter. Always minimize the PCB trace length from the TRIM pin to external components to avoid noise pickup.

Refer to No-Bus™ POL Converters. Z-1000 Series Application Note on www.power-one.com for more application information on this and other product features.

10. Mechanical Drawings

All Dimensions are in mm
Tolerances:
0.5-10 ±0.1
10-100 ±0.2
Pin Coplanarity: 0.1 max

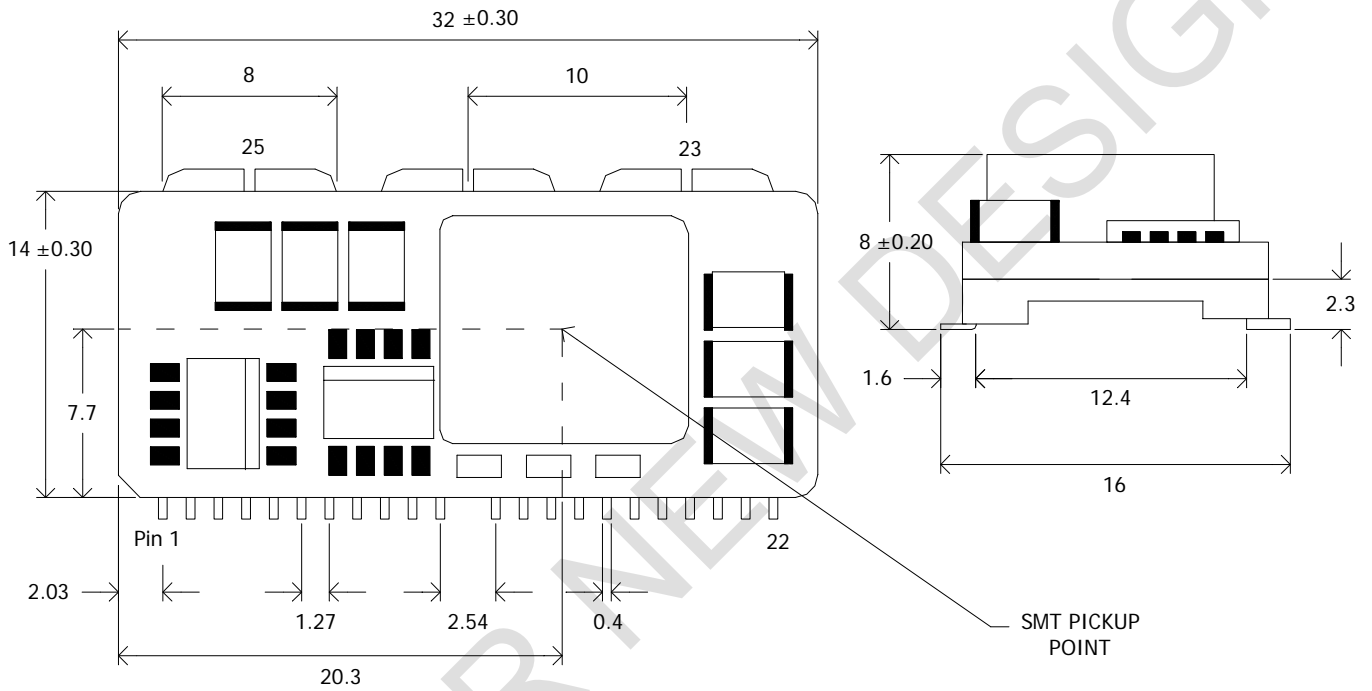


Figure 20. Mechanical Drawing

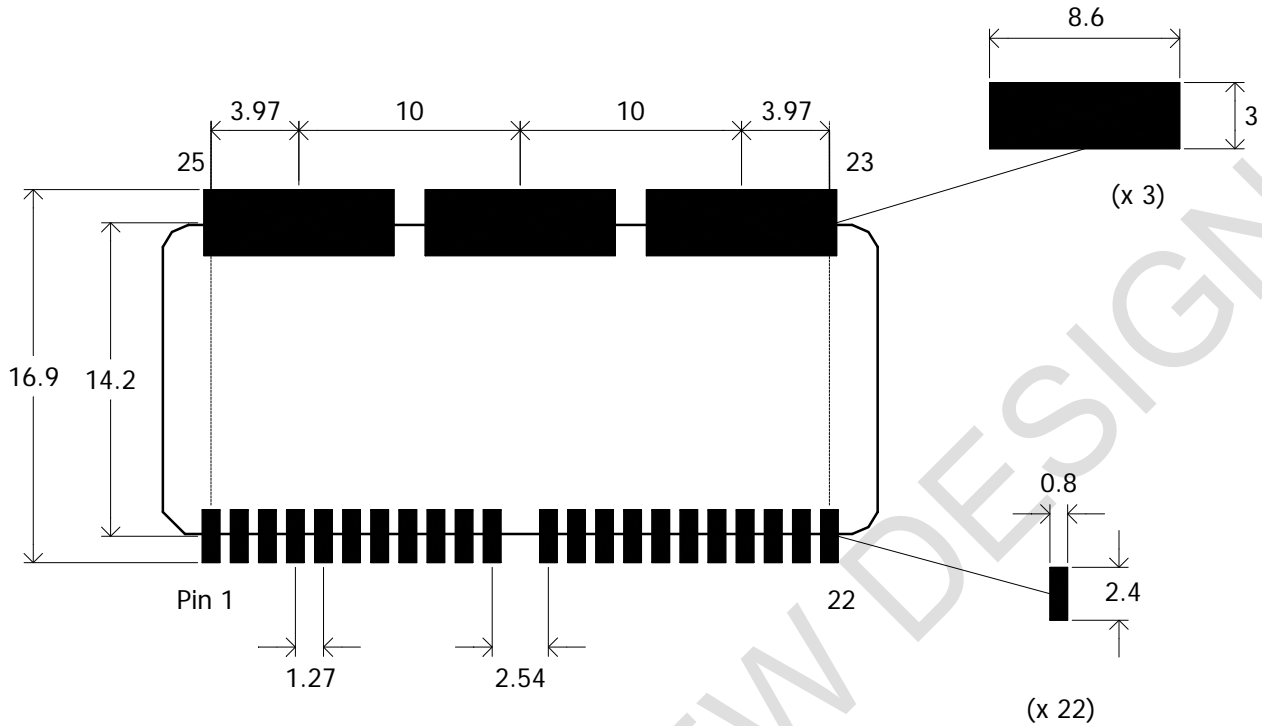


Figure 21. Recommended Pad Sizes

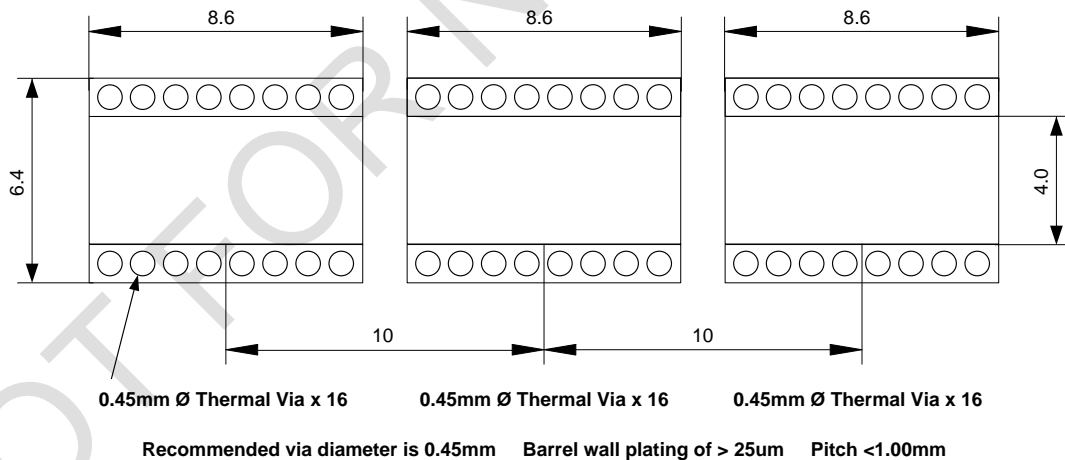


Figure 22. Recommended PCB Layout for Multilayer PCBs

Notes:

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